

In the specification:

Please substitute the following paragraphs for the paragraphs at the indicated locations in the specification as originally filed.

Page 10, line 21+ (twice amended):

Fig. 2 shows the first step taken in forming the invention shown in Fig. 6 from the basic structure shown in Fig. 1. This step includes the deposit of a stressed film 11 (e.g. tensile) over the remaining structure of Fig. 1 in order to produce stress (e.g. tensile) in the channels 201, 211 of the transistors 20 and 21. Prior to the deposit of this film, the sidewall spacers ~~11~~ 10 are optionally removed. The highly stressed film is preferably silicon nitride (Si_3N_4) or silicon oxynitride ($\text{Si}_3\text{O}_x\text{N}_y$) or a combination of both. These materials can be deposited in a highly stressed form providing either tensile or compressional stress, depending on particular process parameters such as plasma power and gas flow rates. For example, using a PECVD process, the stress level is mainly controlled by plasma power and, in general, yields a compressive stress. Thermal CVD Si_3N_4 is deposited at a temperature above 600°C and is normally tensile. Application of this tensile stress enhances the performance of the nMOS transistor 20 while decreasing the performance abilities of the pMOS transistor 21.